Electrical Properties Of Porous Silicon Prepared By Electrochemical Etching Technique

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Abstract

In our work, electrical and optoelectronic properties of P-type porous silicon (PSi) prepared using chemical etching method are studied, specifically capacitance-voltage (C-V), current-voltage (I-V), responsivity and detectivity severally are analyzed. It had been found that electrical characteristics of porous Si samples measured in dark (Id) and below illumination (IPh) will be fitted well by the equations of thermal emission. From this point of view, Schottky barrier height (ϕB) and ideality factor (n) of made-up photodetectors were calculated. The I-V characteristics of dark and illuminations that passes current through the PSi layer reduced by increasing the etching current, as a result of increasing the electrical resistance of PSi layer and therefore the optimum value of ideality factor is (2.7), whereas from C-V characteristic determined that in-built potential accumulated with increasing etching current. The results show that there are clear results for better performance of photodetectors.

Keywords: Porous Silicon, Etching current, Electrical properties, Barrier height, Ideality factor

1. INTRODUCTION

The main focus driven by PSi started in 1990, because of the interest in its development as an efficient light emitting material for optoelectronic applications [1]. PSi classified as a semiconductor material resulting from the electrochemical attack of a strong acid (at most the hydrofluoric acid, HF), in order to create a network of pores with a typical diameter starting from a number of nanometers. Typically this material is observed to be a quantum sponge [2,3]. The anti-reflection and light trappings properties of PSi, as well as its simplicity of reformation and generally tunable morphology make it notably well matched for photovoltaic applications [4]. The interest to review the electrical and photoelectric properties of porous Si layer appears first of all from prospects to developing of the many technological applications like detectors, solar cells, sensors, etc [5].

The current-voltage properties, photovoltaic properties and also the connected the electricity parameters like ideality factor, rectification ratio and therefore the charge carrier mobility mechanisms metal/psi/C-Si/metal sandwich structure rely on

the structural properties of PSi layer [5, 6,7]. However, less work has been done on electrical transport in porous Si devices structures as compared to move in porous Si itself [8].

2 .Experiment part

Porous Si prepared using silicon wafer p-type with (100) orientation and electrical resistance (10 Ω.cm). The substrates were made up of rectangles with areas of (1.5cm × 1.5cm). Then the chemical etching, 0.1 μm thick Al layers were deposited, using the method of an evaporation technique, on the posterior of the wafer. Chemical etching that prepared porous Si exploitation AN electrolyte containing 48th HF and 99.9% surfactants (ethanol) (1:1) for various etching current (7, 9, 11 and 13) mA with mounted etching time (15min) at room temperature as shown in figure (1).

Ethanol is commonly supplemental to facilitate the evacuation of H2 bubbles; these bubbles will simply leave the surface attributable to the reduced surface tension of the liquid. To be capable of synthesizing uniform layers with high reliability, the applied electrode current density and etching time is monitored, controlled and kept at a specific constant level needed throughout the process [9].

Two electrodes are required on the electro-chemical reaction,. the first electrode emit electrons to the solution (Cathode-Au) while the other electrode removes electrons from the solution (Anode - Si wafer). It's necessary notice that the two electrodes are needed to remain charge neutrality and to finish the electric circuit. This implies that a minimum of two reactions are occurring at the same time in an electro-chemical cell, the oxidation reaction and therefore the reduction reaction [10].

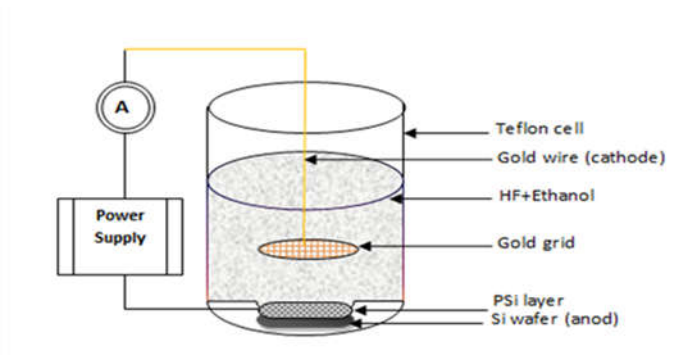

Figure (1): The set-up for preparation of PSi by using ECE process.

3. RESULTS AND DISCUSION

The morphological properties of the PSi samples which it prepared with completely different etching current values (7, 9, 11and 13) mA and etching time at fifteen min as shown in figure (2). Beneath conditions of variable etching current values, the pore morphology was analyzed. At low etching current it's clear there is, an extremely branched, extremely interconnected net and every which way directed of pores were obtained. On the opposite hand, increasing in etching current orders the

little pores to exhibit cylindrical shapes giving rise to a bigger pore diameter of surface pits. Consequently, the surface roughness conjointly will increase (see Table (1)).

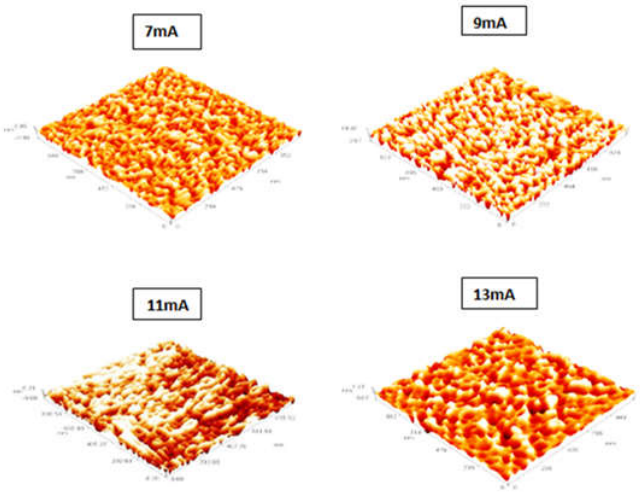

Figure (2): 3D AFM images of p-PSi surface (at 15min and different etching currents)

Table (1): The morphology characteristics of PS samples prepared with different etching currents

Etching current (mA)	*Grain size (nm)*	*Roughens average (nm)*	*Root mean square (nm)*	*Porosity %*
7	27.28	0.167	0.223	34.19
9	33.76	0.572	0.712	49.5
11	50.3	0.736	0.872	68.67
13	68.21	3.05	3.71	75.36

In the figure (3), described (I-V) characteristic of the junction, were obtained by applying a varied the applied bias (from -10V to +10V), for samples ready with etching current (7, 9, eleven and 13) mA and etching times (15 min), within the figure will be explained as within the following observation non-linear behavior (at low voltage), that is mean below the forward bias condition it shows the exponential increase in current. Below reverse bias reverse current is slightly multiplied by the applied voltage and this ends up in generating electron-hole pairs at low bias [11].

The dependence of the I-V characteristics on the etching current is expounded to the formation of pores of PSi, wherever the pore diameter in PSi structure is also accumulated by increasing the etching current, that is diode to increase the electrical resistance of PSi attributable to the carrier caparison at pores wall, that ends up in

reducing the current for all forward biases, attributable to reduced mobility within the progressively PSi layer [12]. The forward current of all photodetector is extremely tiny at a voltage less than two V. This current is understood as recombination current that happens at low voltages only. It's generated once every electron excited from the valence band to induce the balance back. The second region at high voltage represents the diffusion or bending region that looking at serried resistance. In this region, the bias voltage will deliver electrons with enough energy to penetrate the barrier between the two sides of the junction. These results accept as true with the other workers [13].

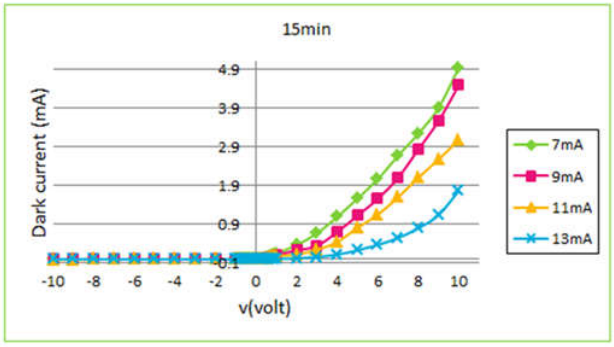

Figure (3): The Current -Voltage characteristics of PSi prepared with different etching current .

It was found that the (I-V) characteristic curves are often fitted well by the subsequent equations of the thermal emission theory[14].

$$I(V) = I_s[\exp\left(\frac{qV}{nKT} - 1\right) \qquad (1)$$

Where V represents the voltage across the device, n is known as the slope parameter or the ideality factor (which is adequate to (1). For the normal Schottky devices, it's a parameter which might show the ideality of made-up devices), K is that the Boltzmann constant and Is is that the saturation current, that obtained from the semi-log forwarded bias as shown in figure (4).

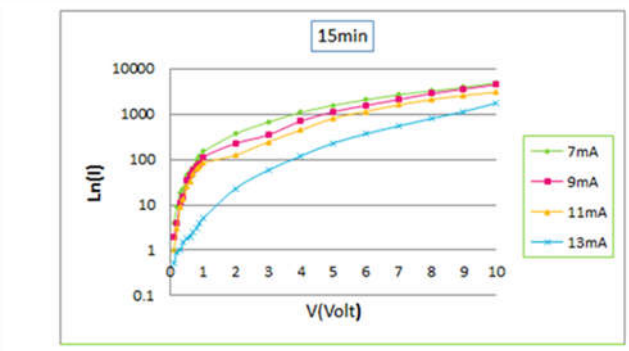

Figure (4): LnI versus V graphic

The barrier height (φB) is often calculated from the following equation [15]:

$$\varphi_B = \frac{KT}{q} ln \frac{A^* AT^2}{I_s} \qquad (2)$$

In Eq. (2), q is that the electron charge, A is that the junction area, A* is that the modified Richardson constant (the theoretical value of A* is 32 Acm-2K-2 for p-type silicon) and (φB) is that the Schottky barrier height. The ideality factor, Schottky barrier height (SBH) for samples are summarized in the table (2).

Table (2): The characteristics of fabricated photodetectors

Etching time	*Etching current (mA)*	*Ideality factor(n)*	$\Phi_{B\,(eV)}$
15min	7	4.2	0.37
	9	3.6	0.36
	11	3.2	0.34
	13	2.7	0.33

From table (2) we have a tendency to observe that the optimum value of ideality factor is (2.7), these results show that increasing the current density could be a way to get an ideal diode, this results sensible agreement with [16], and therefore the barrier height reduced with increasing current density as a result of the interface layer between Ps/c-Si has great amount of pinning, which acts as a defect within the interface and caused to extend saturation current density, thus cause decreasing barrier height of PSi [17].

The Photo-current represented a vital parameter that effected on spectral responsivity, conjointly the} linearity of detector properties also quantum potency. Figure (5) explains the photocurrent characteristics of a sandwich structure below illumination with totally different power densities (330, 1340, 2740 and 5060) μW for samples prepared at completely different etching current (7, 9, 11, and 13) mA and (15min) etching time.

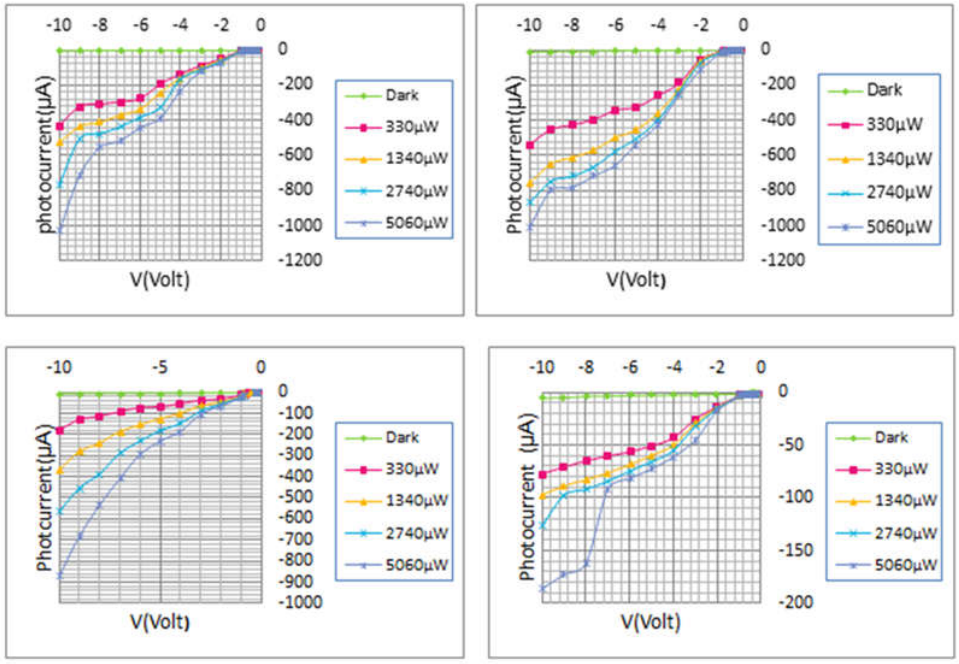

Figure (5): The Photocurrent Density as a function of the applied reverse voltage for Al/PSi/p-Si/Al.

structure device depend upon the morphology and also the porosity of the etched Si surface. Figure (6) shows the C-V characteristics of the sandwich structure with totally different etching current densities (7, 9, 11 and 13) mA, and constant etching time at 15 min.

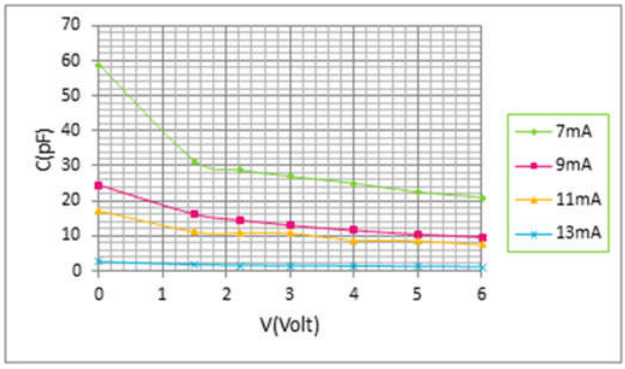

Figure (6): (C-V) characteristics of PSi

The results in Figure (6), shows us that the rise of the etching current density led to decreases the capacitance of the PSi layer and this behavior was attributed to the increase of the depletion region dimension that resulting in the improvement of inbuilt potential [18]. The relation between the inverse capacitance square against the reverse bias is shown in figure (7). This exponential relationship represents that the

junction was an abrupt sort. The spectral responsivity (Rλ) as a function of wavelength (400–950) nm plot for photodetector with 5V bias is given in figure (8).

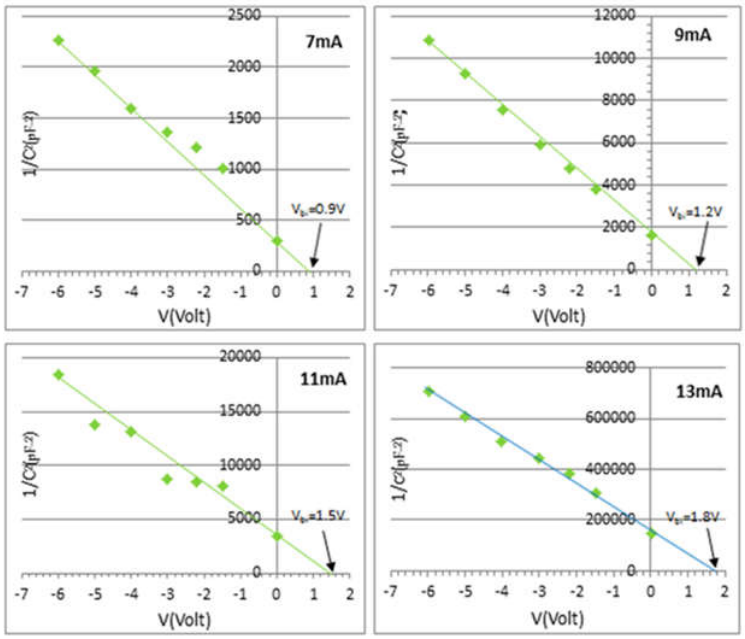

Figure (7): The inverse capacitance squared verses Voltage

The peaks are observed and located at (650, 700, 750 and 800) nm with sensitivities of (0.24, 0.38, 0.61 and 0.69) A/W for samples prepared at 15min and etching current (7,9,11, and 13) mA respectively. The high responsivity of photo-detector is increasing from fact that the porous surface is in caparison photons also because the low concentration of surface recombination which make the surfaces very passivity in addition to the high reflectivity of PSi for light in the visible and near infrared regions is extremely low which agree with [19].

The specific detectivity (D*) of the Al/PSi/p-Si/Al Photodetectors are measured at 25 C0 temperature as a function of light wavelength. Results of D* are illustrated in figure (9) and, the maximal value is about 70× 〖10〗 ^12 cm. 〖Hz〗 ^(1/2) W^(-1) at 800nm.

The maximal values of the specific Detectivity D* are compatible with a result the maximal values of res passivity measure Rλ. The high detectivity of the devices obvious increasing the responsivity as shown in figure (9).The high values of the detectivity big indicator that a good photodetectors is fabricated.

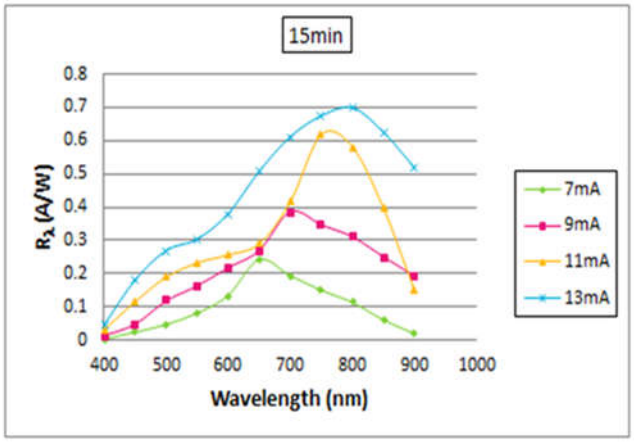

Figure (8): Responsivity Rλ as a function of various incident wavelengths for structure PS/p-Si HJ.

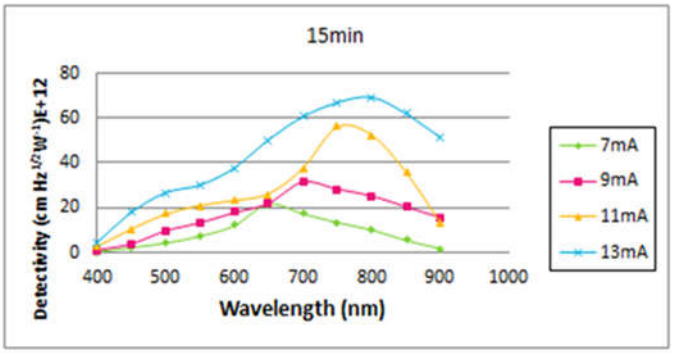

Figure (9): Measured detectivity of the Al/ PS/p-Si/Al photodetector versus wavelength of incident light.

4.CONCLUSION

From our work it is concluded that the electrical properties of Al/psi/c-si/Al sandwich depend on the etching current and this due to the nano size of porous Si and also the varied of the porosity and layer thickness of the porous Si causes increasing within the current resistance and this result in different current density. The C-V characteristics show that the rise of the current density decreases the capacitance of the PSi layer. This behavior was attributed to the increase within the depletion region dimension that resulting in the increasing of intrinsic potential. The photodetector has sensible linearity characteristics and shows a good photoresponse in each visible and near IR regions, with a sensitivity of 0.69 A/W at 800 nm. The barrier height isn't close to zero, so a rectifying contact is expected. Once a forward bias was applied to the metal-semiconductor junction the electron energy levels on the semiconductor side can increase by e(Vbi –VF), wherever VF (Volt) denotes the applied forward bias voltage between metal and semiconductor. Therefore, the Fermi energy state of

the semiconductor ought to increase by the value of ev in addition. Thus, barrier height for the electrons passing from semiconductor to metal will be small by ev.

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